15. An electronic device comprising:

at least one central processing unit; and

a glitch detector configured to generate a clock corresponding to a power voltage, to count the clock to generate a count value, to compare a reference value with the count value, to generate an alarm signal based on a result of the comparison, and to output the alarm signal to the at least one central processing unit,

wherein the at least one central processing unit is configured to perform a reset operation in response to the alarm signal.

16. The electronic device of claim **15**, wherein the reference value comprises an upper limit and a lower limit.

17. The electronic device of claim **16**, wherien the at least one central processing unit is configured to change the upper limit and the lower limit.

18. The electronic device of claim **15**, wherein the glitch detector is configured to generate the alarm signal when an absolute value of the count value minus the moving average value is greater than a threshold value.

19. The electronic device of claim **15**, wherein the glitch detector is configured to generate the alarm signal when the count value is greater than the moving average value, and the count value is greater than an upper limit, or

wherein the glitch detector is configured to generate the alarm signal when the count value is not greater than the moving average value, and the count value is less than a lower limit.

20-29. (canceled)

30. A glitch detector comprising:

a clock generator configured to generate a clock signal having a frequency that varies based on a power voltage driving the clock generator; and

at least one processor configured to count the clock signal, and to output an alarm when the count is outside a limit.

31-35. (canceled)

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